



FIG. 1

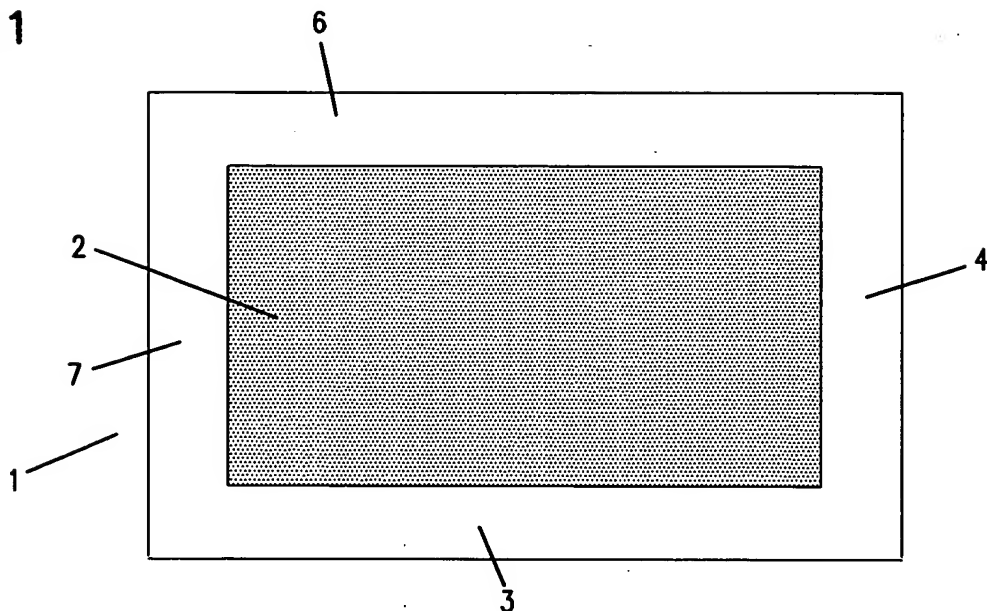
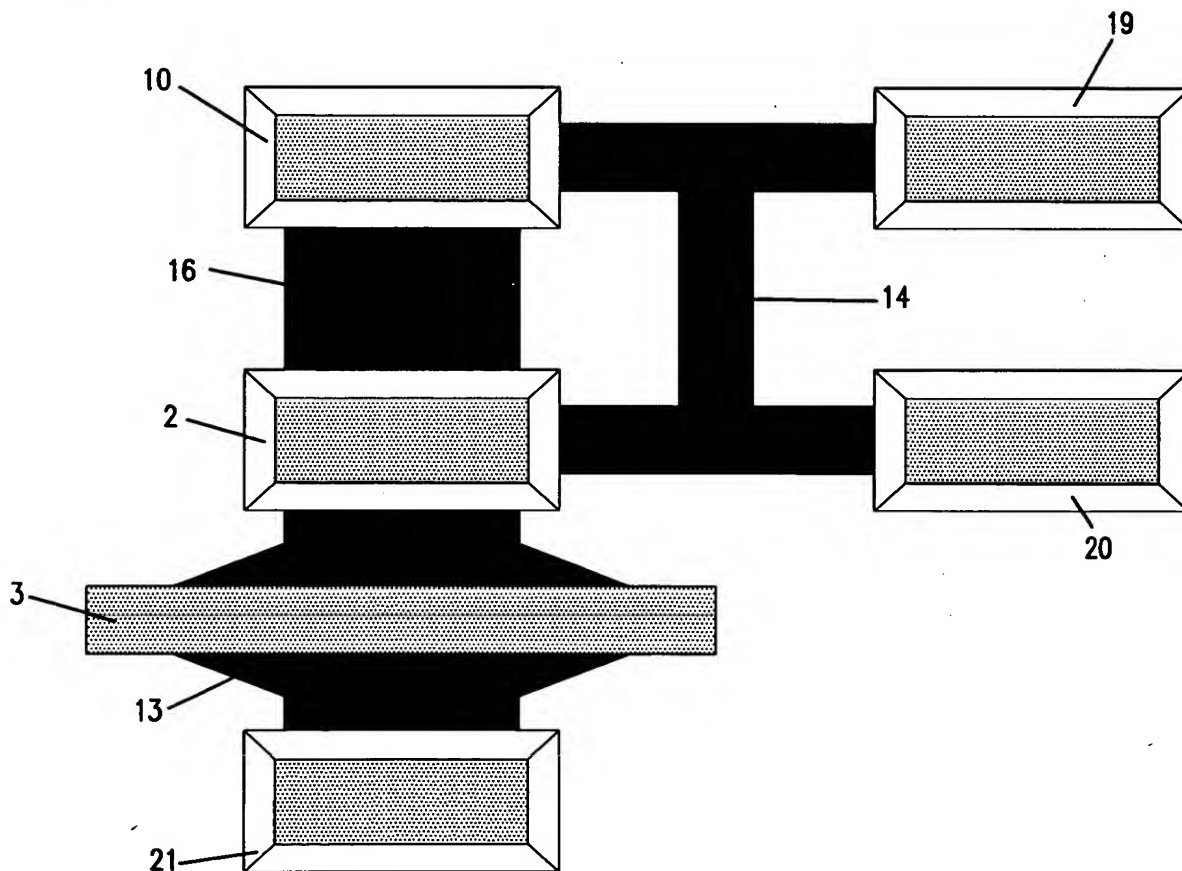
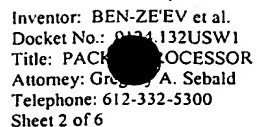


FIG. 2





The diagram illustrates a system architecture with a central **R-BUS** (44) acting as a hub. The components and their connections are as follows:

- PHY I/F** (40): Connected to the R-BUS via a bidirectional interface.
- FIFO 6** (63) and **FIFO 4** (62): Part of a dashed block (24) on the left. They are connected to a large rectangular block (22) via thick arrows. A thick arrow (1) exits the top of block 22, and a thick arrow (29) enters the bottom of block 22.
- FIFO 1** (60) and **FIFO 3** (61): Part of a dashed block (23) on the right. They are connected to a large rectangular block (21) via thick arrows. A thick arrow (23) exits the top of block 21, and a thick arrow (61) enters the bottom of block 21.
- 6 X DMA** (27): Connected to the R-BUS via a bidirectional interface. It also has a thick arrow (29) entering from the left and a thick arrow (46) exiting to the right.
- PCI INTERFACE** (25) and **PCI INTERFACE** (26): Connected to the 6 X DMA (27) via bidirectional interfaces.
- Internal R-BUS Components**: Inside the R-BUS (44) are a **TIMER** (65) and **EXTERNAL INTERFACES (JTAG, 12C...)** (66), both connected to the R-BUS via bidirectional interfaces.



FIG. 4

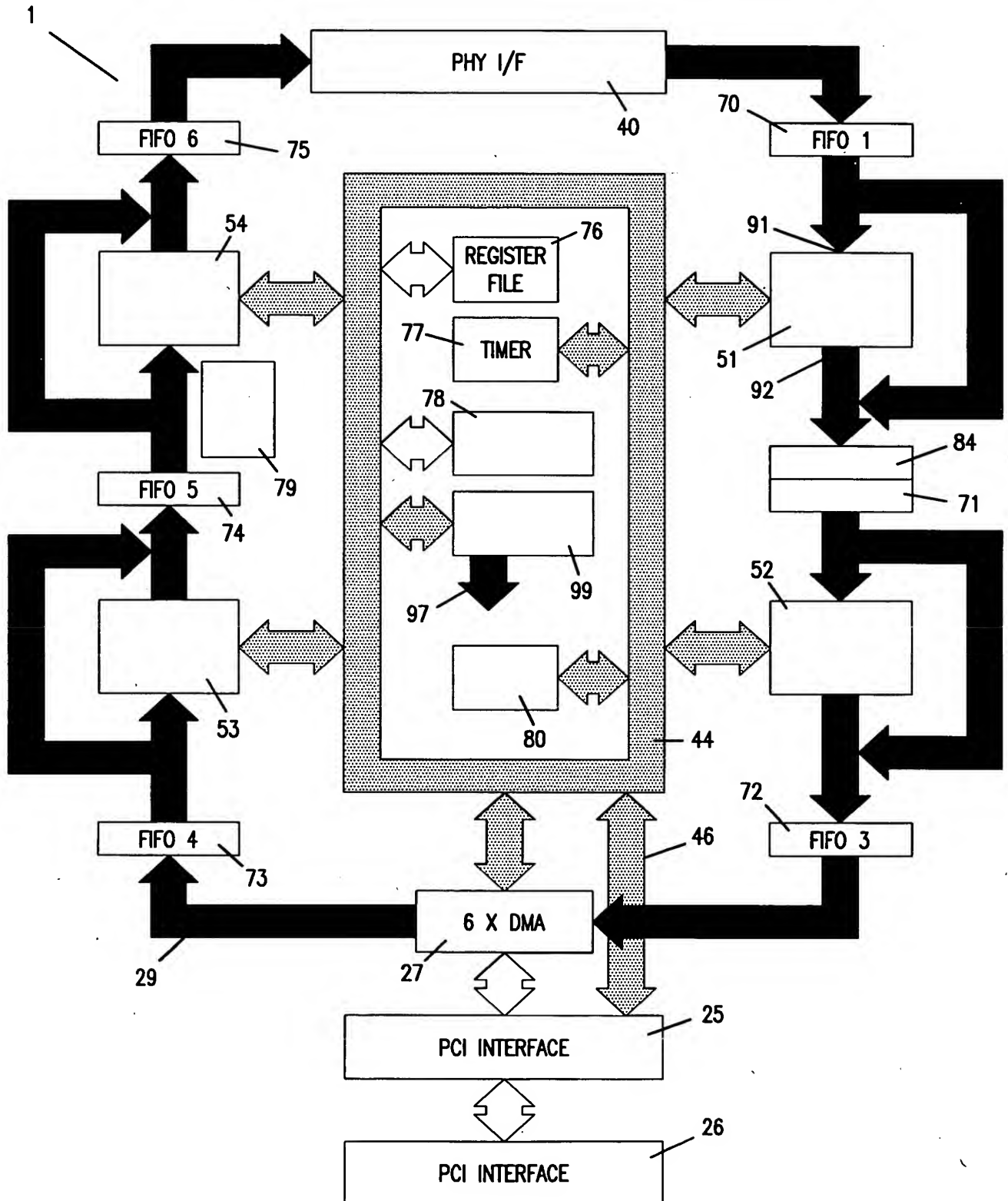
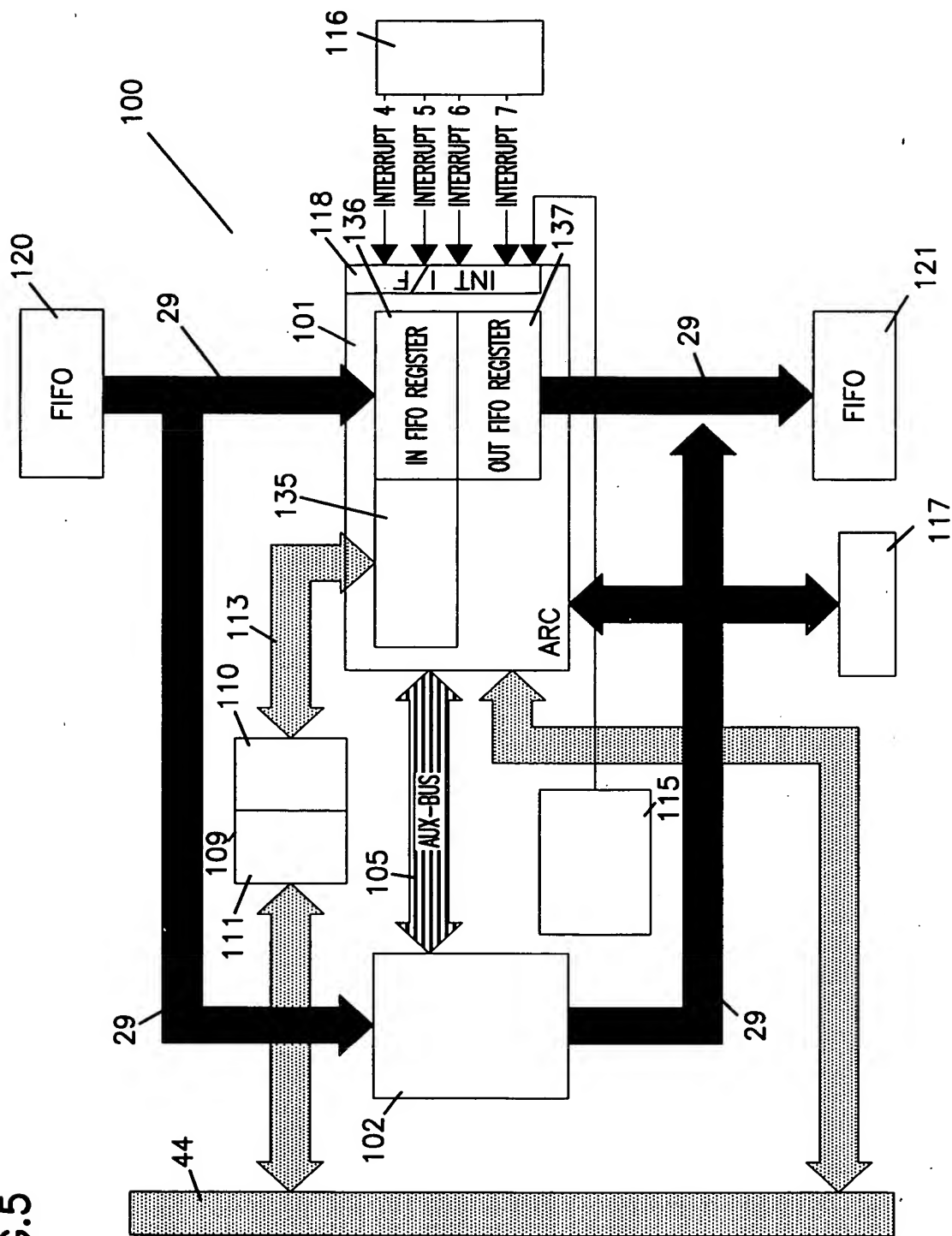




FIG. 5



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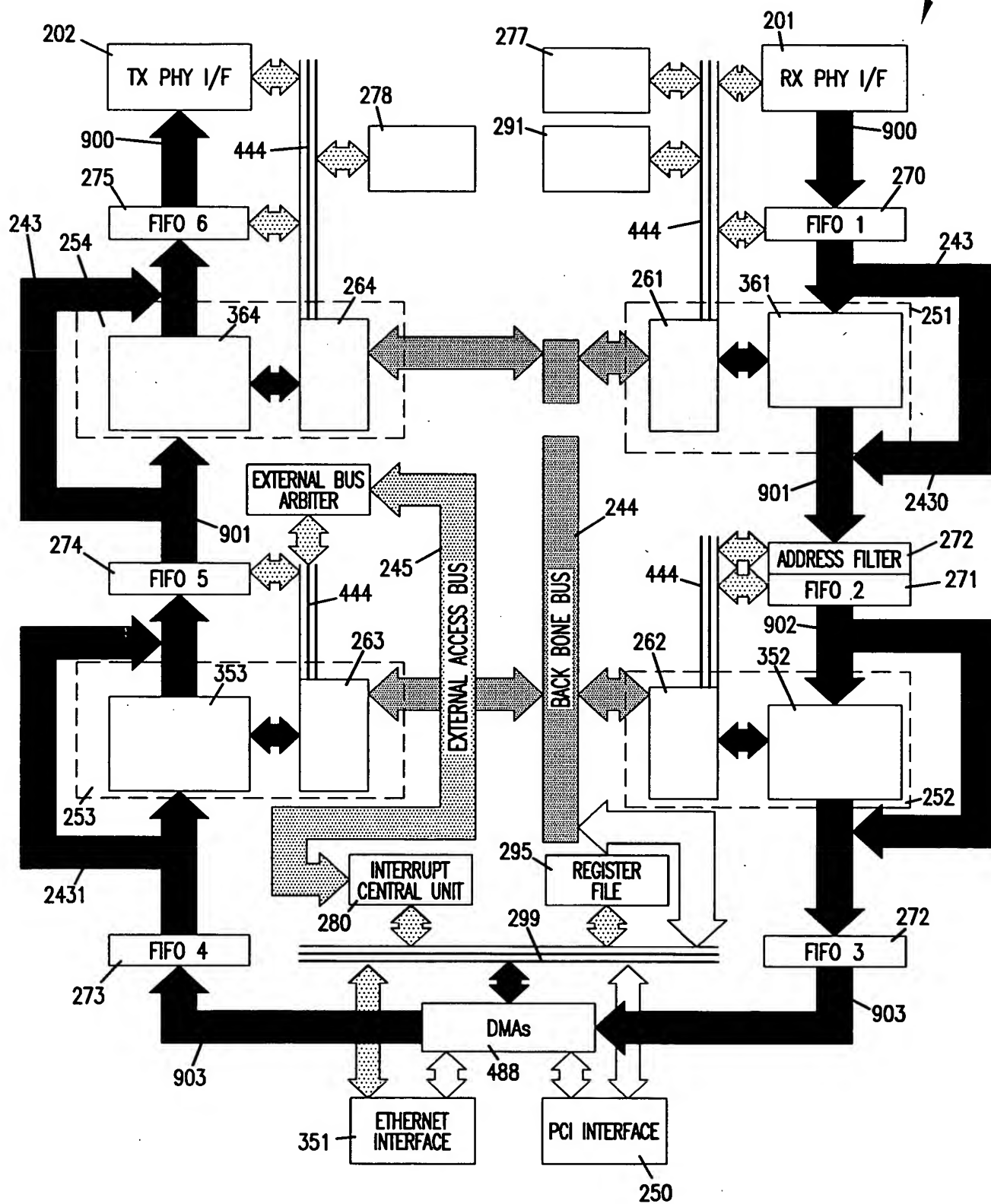




FIG. 7

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